What is claimed is:

1. A method of design rule checking an integrated circuit, comprising:

identifying any line having a line width marker and line width parameter;

extracting each line having a line width marker;

determining the line width parameter for each extracted line; and

comparing the line width parameter with an actual line width for the line.

2. The method of claim 1, wherein extracting excludes lines near or above a transistor.

3. The method of claim 1, and further comprising generating an error condition when the actual line width for the line is less than the line width parameter.

4. The method of claim 1, and further comprising indicating or recording an error when the actual line width for the line is less than the line width parameter.

5. The method of claim 1, wherein each line having a width marker has a width greater than a minimum width for that line.

6. The method of claim 1, wherein identifying any line comprises identifying any line in a schematic.

7. The method of claim 1, wherein each extracted line has a line width marker in a layout.

8. The method of claim 1, wherein each extracted line has a line width marker in a line width layer.

9. The method of claim 1, wherein the line width parameter represents a minimum line width for the line associated with that line width parameter.

10. The method of claim 1, and further comprising extracting a width for each extracted line.

11. The method of claim 1, wherein determining the line width parameter for each extracted line comprises extracting the line width marker and line width parameter for each extracted line.

12. A method of design rule checking an integrated circuit, comprising:

identifying any line having a line width marker and line width parameter;

excluding the line if it is near or above a transistor;

extracting each line having a line width marker;

determining the line width parameter for each extracted line; and

comparing the line width parameter with an actual line width for the line.

13. The method of claim 12, and further comprising generating an error condition when the actual line width for the line is less than the line width parameter.

14. The method of claim 12, wherein determining the line width parameter for each extracted line comprises extracting the line width marker and line width parameter for each extracted line.

15. The method of claim 12, wherein identifying any line comprises identifying that line in a schematic.

16. A method of design rule checking an integrated circuit, comprising:

identifying any line having a line width marker and line width parameter;

extracting each line having a line width marker;

determining the line width parameter for each extracted line;

comparing the line width parameter with an actual line width for the line; and

excluding from comparing any portion of the line near or above a transistor.

17. The method of claim 16, and further comprising indicating or recording an error when the actual line width for the line is less than the line width parameter.

18. The method of claim 16, wherein determining the line width parameter for each extracted line comprises extracting the line width marker and line width parameter for each extracted line.

19. The method of claim 16, wherein identifying any line comprises identifying that line in a schematic.